In the claims:

For the Examiner's convenience, all pending claims are presented below with changes shown in accordance with the mandatory amendment format.

1   1.   (Currently Amended) A computer system comprising:

2   a central processing unit (CPU); and

3   a cache memory, coupled to the CPU, having a plurality of compressible cache

4   lines to store additional data; and

5   a cache controller to perform lookup operations of the cache memory, the cache

6   controller having an array of tag entries corresponding to each of the plurality of cache

7   lines, each tag entry including:

8   address tag bits corresponding to a cache line address;

9   one or more compression encoding bits indicating whether a

10   corresponding cache line is compressed; and

11   one or more companion encoding bits indicating which companion lines

12   are stored in a common cache set, wherein if the compression bit indicates the

13   cache line is compressed the companion bit is <u>disregarded</u> ~~treated as a part of an~~

14   ~~offset~~ and if the compression bit indicates the cache line is not compressed the

15   companion bit is compared with a tag ~~considered a component of the address tag~~

16   ~~bits~~.

1   2.   (Cancelled)

1   3.   (Original)   The computer system of claim 1 wherein the cache controller is

2   included within the CPU.

1   4.   (Cancelled)

1   5.   (Currently Amended) The computer system of claim 1 [[4]] wherein the cache

2   line stores two or more cache lines if the corresponding compression bit indicates that the

3   line is compressed.

1   6.   (Cancelled)

1   7.   (Original)   The computer system of claim 5 wherein the companion lines are

2   adjacent memory lines.

1   8.   (Currently Amended) The computer system of claim 1 [[4]] wherein the

2   companion encoding bits are used as a compression format bit to select between different

3   compression algorithms.

1   9.   (Currently Amended) The computer system of claim 1 [[4]] wherein the

2   companion encoding bits are used to encode the ordering of companion lines in the

3   compressed line.

1   10.   (Previously Presented)   The computer system of claim 1 wherein the cache

2   controller further comprises set and way selection logic to select a cache line.

1   11.   (Previously Presented)   The computer system of claim 10 wherein the set

2   and way selection logic comprises tag comparison logic to compare the cache line

3   address to the address tag bits.

1   12.   (Original)   The computer system of claim 11 wherein the tag comparison logic

2   ignores the one or more companion encoding bits within the address if the one or more

3   compression encoding bits indicate that the cache line is compressed.

1   13.   (Previously Presented)   The computer system of claim 11 wherein the tag

2   comparison logic compares ~~the~~ one or more companion bits within the address with the

3   one or more companion encoding bits within the tag if the compression encoding bits

4   indicate that the cache line is not compressed.

1   14.   (Original)   The computer system of claim 10 wherein the cache controller

2   further comprises compression logic to compress a cache line.

1   15.   (Original)   The computer system of claim 14 wherein the compression logic

2   compresses cache lines via a dictionary based compression algorithm.

1   16.   (Original)   The computer system of claim 14 wherein the compression logic

2   compresses cache lines via a sign-bit compression algorithm.

1   17.   (Original)   The computer system of claim 14 wherein the compression logic

2   determines when a cache line is to be compressed.

1   18.   (Original)   The computer system of claim 17 wherein the compression logic

2   compresses a cache line based upon opportunistic compression.

1   19.   (Original)   The computer system of claim 17 wherein the compression logic

2   compresses a cache line based upon prefetch compression.

1   20.   (Original)   The computer system of claim 17 wherein the compression logic

2   compresses a cache line based upon victim compression.

1   21.   (Original)   The computer system of claim 14 wherein the cache controller

2   further comprises byte selection logic to select addressed datum within a cache line.

1   22.   (Original)   The computer system of claim 21 wherein the byte selection logic

2   comprises:

3   a decompressor to decompress a selected cache line;

4   an input multiplexer to select between a decompressed cache line and an un-

5   decompressed cache line; and

6   an output multiplexer to select between companion lines in the uncompressed

7   cache line.

1   23.   (Currently Amended) A cache controller comprising:

2   compression logic to compress lines within a cache memory device; and

3   an array of tag entries corresponding to each of a plurality of cache lines, each tag

4   entry including:

5   address tag bits corresponding to a cache line address;

6   one or more compression encoding bits indicating whether a

7   corresponding cache line is compressed; and

8   one or more companion encoding bits indicating which companion lines

9   are stored in a common cache set, wherein if the compression bit indicates the

10   cache line is compressed the companion bit is <u>disregarded</u> ~~treated as a part of an~~

11   ~~offset~~ and if the compression bit indicates the cache line is not compressed the

12   companion bit is compared with a tag ~~considered a component of the address tag~~

13   ~~bits~~.

1   24.   (Previously Presented)   The cache controller of claim 23 further comprising

2   set and way logic to select from a plurality of cache lines.

1   25.   (Previously Presented)   The cache controller of claim 23 ~~24~~ wherein a

2   single cache line stores two or more cache lines if the corresponding compression bit

3   indicates that the line is compressed.

1   26.   (Cancelled)

1   27.   (Previously Presented)   The cache controller of claim 24 wherein the set

2   and way selection logic comprises tag comparison logic to compare ~~a~~ the cache line

3   address to the address tag bits.

1   28.   (Currently Amended) The cache controller of claim 27 wherein the tag

2   comparison logic ignores the one ~~ore~~ <u>or</u> more companion encoding bits within the

3   address if the one or more compression encoding bits indicate that the cache line is

4   compressed.

1   29.   (Currently Amended) The cache controller of claim 28 wherein the tag

2   comparison logic compares one or more companion bits within the address with the one

3   ore or more companion encoding bits within the tag if the compression encoding bits

4   indicates that the cache line is not compressed.

1   30.   (Original)   The cache controller of claim 23 wherein the compression logic

2   compresses cache lines via a dictionary based compression algorithm.

1   31.   (Original)   The cache controller of claim 23 wherein the compression logic

2   compresses cache lines via a sign-bit compression algorithm.

1   32.   (Original)   The cache controller of claim 23 wherein the compression logic

2   determines when a cache line is to be compressed.

1   33.   (Original)   The cache controller of claim 23 wherein the cache controller

2   further comprises byte selection logic to select addressed datum within a cache line.

1   34.   (Original)   The cache controller of claim 33 wherein the byte selection logic

2   comprises:

3   a decompressor to decompress a selected cache line;

4   an input multiplexer to select between a decompressed cache line and an un-

5   decompressed cache line; and

6   an output multiplexer to select between companion lines in the uncompressed

7   cache line.

1   35.   (Previously Presented)   A method comprising:

2   analyzing a tag associated with a first cache line in a tag array to determine if the

3   first cache line is compressed;

4   analyzing one or more companion encoding bits if the first cache line is not

5   compressed; and

6   disregarding the one or more companion encoding bits if the first cache line is

7   compressed.

1   36.   (Previously Presented)   The method of claim 35 wherein compressing the

2   first cache line comprises storing data from a second cache line within the first cache line.

1   37.   (Previously Presented)   The method of claim 35 further comprising

2   determining if a first cache line within a cache memory device is to be compressed.

1   38.   (Previously Presented)   The method of claim 37 further comprising

2   compressing the first cache line.

1   39.   (Cancelled)

1   40.   (Previously Presented)   The method of claim 35 further comprising using

2   the one or more companion encoding bits as a compression format bit to select between

3   different compression algorithms if the first cache line is compressed.

1   41.   (Currently Amended) The method of claim 35 37 further comprising using the

2   one or more companion encoding bits to encode the ordering of companion lines in the

3   first cache line if the first cache line is compressed.

1   42.   (Currently Amended) A computer system comprising:

2   a central processing unit (CPU);

3   a cache memory, coupled to the CPU, having a plurality of compressible cache

4   lines to store additional data;

5   a cache controller to perform lookup operations of the cache memory, the cache

6   controller having an array of tag entries corresponding to each of the plurality of cache

7   lines, each tag entry including:

8   address tag bits corresponding to a cache line address;

9   one or more compression encoding bits indicating whether a

10   corresponding cache line is compressed; and

11   one or more companion encoding bits indicating which companion lines

12   are stored in a common cache set, wherein if the compression bit indicates the

13   cache line is compressed the companion bit is disregarded treated as a part of an

14   offset and if the compression bit indicates the cache line is not compressed the

15   companion bit is compared with a tag considered a component of the address tag

16   bits;

17   a chipset coupled to the CPU; and

18   a main memory.

1 43. (Cancelled)

1 44. (Currently Amended) The computer system of claim 42 ~~1~~ wherein the cache

2 controller is included within the CPU.

1 45. (Currently Amended) The computer system of claim 42 ~~1~~ wherein the cache

2 controller is included within the chipset.

1 46. (Cancelled)

1 47. (Previously Presented)   The computer system of claim 42 wherein a single

2 cache line stores two or more cache lines if the corresponding compression bit indicates

3 that the line is compressed.